100Gbps QSFP28 ER4 Lite OTU4 Optical Transceiver Module

QSFP28-100G-ER4-30K-D

FEATURES

- 4 channels full-duplex transceiver modules
- Supports data rate up to 111.8Gb/s
- Supports QSFP28 4WDM 40km MSA/100GBASE-ER4 Lite/OTU4
- 4 x 28Gb/s DFB-based LAN-WDM Cooling transmitter
- 4 channels APDROSA
- Internal CDR circuits on both receiver and transmitter channels
- Low power consumption<3.8W
- Hot Pluggable QSFP form factor
- Up to 30kmreachfor G.652 SMF without FEC
- Up to 40kmreach for G.652 SMF with FEC
- Duplex LC receptacles
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 6 compliant (lead free)

APPLICATIONS

- IEEE 802.3ba 100GBASE ER4 Links
- Client-side 100G interconnections
- OTN OTU4

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{cc}	-0.3	3.6	V
Input Voltage	V_{in}	-0.3	V_{cc}+0.3	V
Storage Temperature	T_s	-20	85	°C
Case Operating Temperature	T_c	0	70	°C
Humidity (non-condensing)	Rh	5	85	%
Damage Threshold (each lane)	TH_d	5.5		dBm

INDONESIA OFFICE (NEW)
WEST PARK B-23
JL. BLVD. BARAT BSD CITY
PAGEDANGAN, TANGERANG
BANTEN 15336
+62 2 150 858 721

HEAD OFFICE AND R&D LAB
UNIT 1 / 6 POWELLS ROAD
BROOKVALE, SYDNEY
NSW 2100 AUSTRALIA
+61 2 8078 2207

MELBOURNE OFFICE
11 CORPORATE DRIVE
CRANBOURNE WEST
VIC 3977 AUSTRALIA
+61 3 8679 4575

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case Temperature	Tc	0		70	°C
Data Rate Per Lane	fd		25.78125		Gb/s
Humidity	Rh	5		85	%
Power Dissipation	Pm		3.5	3.8	W
Link Distance with G.652	D	0.002		40	km

DIAGNOSTIC MONITORING INTERFACE

Parameter	Symbol	Min.	Max.	Unit	Note
Temperature Monitor Absolute Error	DMI_Temp	-3	3	°C	1
Supply Voltage Monitor Absolute Error	DMI _V_{cc}	-0.1	0.1	V	2
Channel RX Power Monitor Absolute Error	DMI_RX_Ch	-7	-22	dB	3
Channel Bias Current Monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX Power Monitor Absolute Error	DMI_TX_Ch	-2.5	6.5	dB	3

Note:

1. Over operating temperature range.
2. Over full operating range.
3. Due to measurement accuracy of different single mode fibres, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

TRANSMITTER ELECTRO-OPTICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Current	Icc			1.27	A	-
Power Consumption	P			4.2	W	
Transceiver Power-on Initialization Time				2000	ms	
Single-ended Input Voltage Tolerance		-0.3		4.0	V	-
AC Common Mode Input Voltage Tolerance		15			mV	-
Differential Input Voltage		50			mVp-p	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note

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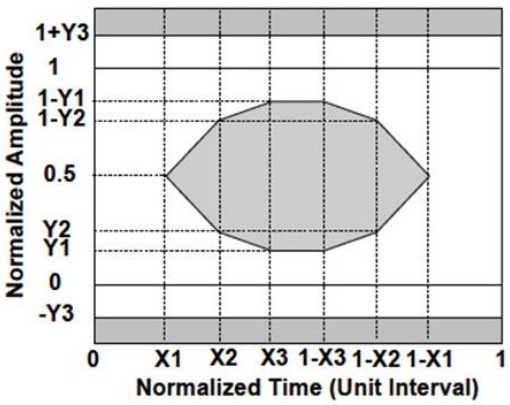
Differential Input Voltage Swing	Vin			900	mVp-p	-
Differential Input Impedance	Zin	90	100	110	Ohm	-
Lane Wavelength	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.19	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	PT			12.5	dBm	
Average Launch Power (each lane)	P_{AVG}	-2.5		6.5	dBm	
Optical Modulation Amplitude (each lane)	P_{OMA}	0.5		6.5	dBm	2
Difference in Launch Power	$P_{tx,diff}$			3	dB	
Launch Power in OMA minus TDP		-0.5			dBm	
Transmitter and Dispersion Penalty (TDP) (each lane)	TDP			3.0	dB	
Extinction Ratio	ER	4.5			dB	
Relative Intensity Noise	RIN			-130	dB/Hz	
Optical Return Loss Tolerance	T_{OL}			20	dB	
Transmitter Reflectance	R_T			-12	dB	
Average Launch Power of OFF transmitter (each lane)	P_{OFF}			-30	dBm	
Eye Mask Coordinates: X1, X2, X3, Y1, Y2, Y3	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}					3

Note:

1. Power-on Initialization Time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.
2. Even if the TDP <1dB, the OMA min must exceed the minimum value specified here.
3. See figure below



RECEIVER ELECTRO-OPTICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Single-ended Output Voltage		-0.3		4.0	V	
AC Common Mode Output				7.5	mV	
Differential Output Voltage Swing	V_{out}	300		850	mVp-p	
Differential Output Impedance	Z_{out}	90	100	110	Ohm	
Damage Threshold (each lane)	TH_d	-6			dBm	1
Average Receive Power (each lane)		-20.5		-7	dBm	
Receive Power (OMA) (each lane)				-7	dBm	
Receiver Sensitivity (OMA) (each lane) (BER = 5×10^{-5})	SEN1			-18.5	dBm	@100GE
Receiver Sensitivity (OMA) (each lane) (BER = 5×10^{-12})	SEN2			-15	dBm	@100GE
Stressed Receiver Sensitivity (OMA)4	SEN3			-16	dBm	2
Receiver Sensitivity (OMA) (each lane) (BER = 5×10-12) @OTU4	SEN4			-18	dBm	@OTU4
Receiver Sensitivity (OMA)	SEN5			-14	dBm	@OTU4
Difference in Receive Power between any Two Lanes (OMA)	$P_{rx,diff}$			3.6	dB	
LOS Assert			-26		dBm	
LOS De-Assert – OMA			-24		dBm	
LOS Hysteresis	0.5				dB	
Receiver Electrical 3 dB upper Cut-off Frequency (each Lane)	Fc			31	GHz	

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WEST PARK B-23
JL. BLVD. BARAT BSD CITY
PAGEDANGAN, TANGERANG
BANTEN 15336
+62 2 150 858 721

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UNIT 1 / 6 POWELLS ROAD
BROOKVALE, SYDNEY
NSW 2100 AUSTRALIA
+61 2 8078 2207

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11 CORPORATE DRIVE
CRANBOURNE WEST
VIC 3977 AUSTRALIA
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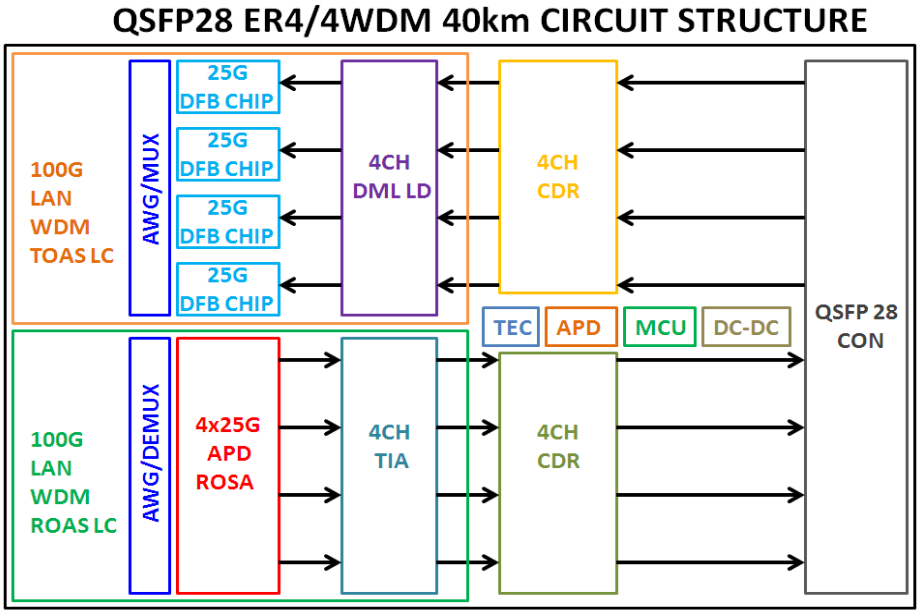
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Conditions of Stress Receiver Sensitivity Test (Note 3)						
Vertical Eye Closure Penalty, each Lane			2.5		dB	3
Stressed Eye J2 Jitter, each Lane			0.33		UI	
Stressed Eye J9 Jitter, each Lane			0.48		UI	

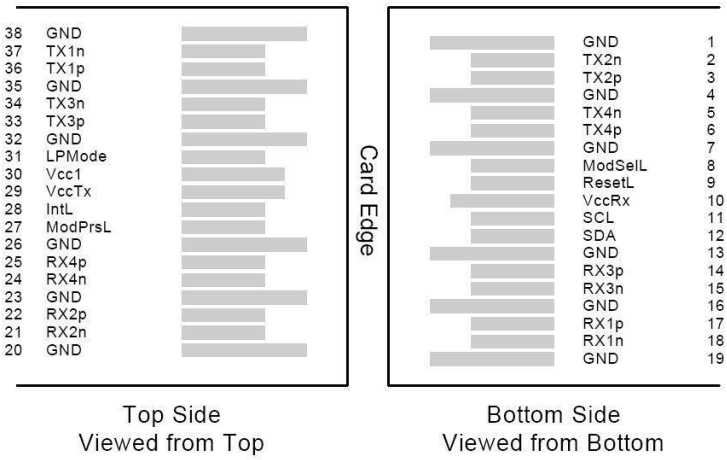
Note:

1. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
2. Measured with conformance test signal at receiver input for BER = 5x10-5 @25.78125Gbps.
3. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

BLOCK DIAGRAM



PIN ASSIGNMENT



Top Side
Viewed from Top

Bottom Side
Viewed from Bottom

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UNIT 1 / 6 POWELLS ROAD
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NSW 2100 AUSTRALIA
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ModSelL PIN

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

Cloudtron QSFP28 modules operate in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and de-asserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

PIN DESCRIPTION

PIN	Logic	Symbol	Name/Description	Note
1		GND	Module Ground	1
2	CML-I	Tx2-	Transmitter inverted data input	
3	CML-I	Tx2+	Transmitter non-inverted data input	
4		GND	Module Ground	1
5	CML-I	Tx4-	Transmitter inverted data input	
6	CML-I	Tx4+	Transmitter non-inverted data input	
7		GND	Module Ground	1
8	LVTTL-I	MODSEIL	Module Select	2
9	LVTTL-I	ResetL	Module Reset	2
10		VCCRx	+3.3V Receiver Power Supply	
11	LVCMOS-I	SCL	2-wire Serial interface clock	2
12	LVCMOS-I/O	SDA	2-wire Serial interface data	2
13		GND	Module Ground	1
14	CML-O	RX3+	Receiver non-inverted data output	
15	CML-O	RX3-	Receiver inverted data output	
16		GND	Module Ground	1
17	CML-O	RX1+	Receiver non-inverted data output	
18	CML-O	RX1-	Receiver inverted data output	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-O	RX2-	Receiver inverted data output	
22	CML-O	RX2+	Receiver non-inverted data output	
23		GND	Module Ground	1
24	CML-O	RX4-	Receiver inverted data output	
25	CML-O	RX4+	Receiver non-inverted data output	
26		GND	Module Ground	1
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND	
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board	2
29		VCCTx	+3.3V Transmitter Power Supply	
30		VCC1	+3.3V Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Module Ground	1
33	CML-I	Tx3+	Transmitter non-inverted data input	

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PIN	Logic	Symbol	Name/Description	Note
34	CML-I	Tx3-	Transmitter inverted data input	
35		GND	Module Ground	1
36	CML-I	Tx1+	Transmitter non-inverted data input	
37	CML-I	Tx1-	Transmitter inverted data input	
38		GND	Module Ground	1

Note:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.

TIMING FOR SOFT CONTROL AND STATUS FUNCTIONS

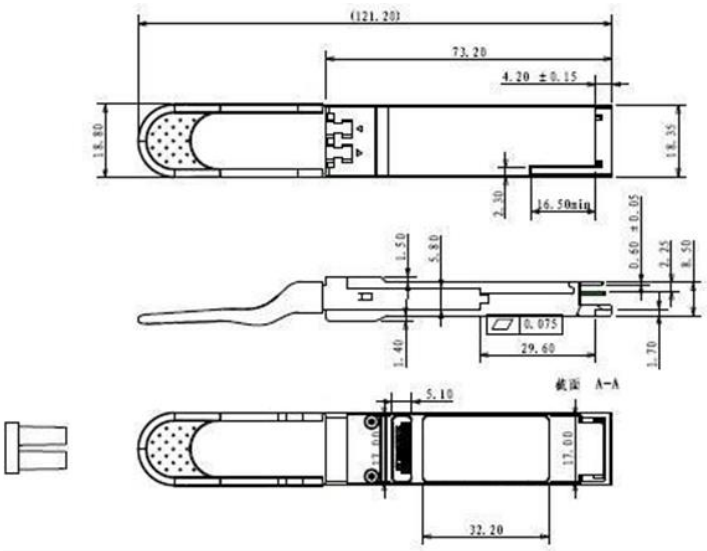
Parameter	Symbol	Max	Unit	Condition
Initialization Time	t_init	2000	ms	Time from power on1, hot plug or rising edge of Reset until the module is fully functional2
Reset Init Assert Time	t_reset_init	2	µs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on1 until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on1 to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional2
LPMode Assert Time	ton_LPMode	100	µs	Time from assertion of LPMode (Vin: LPMode=VIH) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout: IntL=VOL
IntL Deassert Time	toff_IntL	500	µs	Time from clear on read3 operation of associated flag until Vout: IntL=VOH. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted

Parameter	Symbol	Max	Unit	Condition
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set4 until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared4 until associated IntlL operation resumes
ModSelL Assert Time	ton_ModSelL	100	μs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial
ModSelL Deassert Time	toff_ModSelL	100	μs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2- wire serial bus
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set4 until module power consumption enters lower Power Level
Power_over-ride or Power-set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared4 until the module is fully functional3

Note：

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

DIMENSIONS



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