QSFP28-100G-ZR4

100Gb/s QSFP28 ZR4 Transceiver

Product Features

- Compliant with QSFP28 Standard: SFF-8661 Rev 2.5, SFF-8636 Rev 2.10a
- High speed I/O electrical interface (CAUI-4) compliant with IEEE 802.3bm-2015
- 100GBASE-ZR4 point-to-point Ethernet links Rx sensitivity of -28dBm with enabled KR4 FEC in host for up to 80km SMF
- Single 3.3V Supply Voltage
- Maximum power consumption 5.5W
- 0-70 ºC Case Operating Temperature
- LAN WDM EML laser and SOA+PIN Receiver
- Universal QSFP28 MSA package with duplex LC connector
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant) Class 1 Laser

INDONESIA OFFICE NEW
WEST PARK B-23
JL. BLVD. BARAT BSD CITY
PAGEDANGAN, TANGERANG
BANTEN 15336
+62 2 150 858 721

HEAD OFFICE AND R&D LAB
UNIT 1 / 6 POWELLS ROAD
BROOKVALE, SYDNEY
NSW 2100 AUSTRALIA
+61 2 8078 2207

MELBOURNE OFFICE
11 CORPORATE DRIVE
CRANBOURNE WEST
VIC 3977 AUSTRALIA
+61 3 8679 4575

USA R&D LAB
48233
WARM SPRINGS BLVD.
FREMONT CA
+1 510 945 1001
+1 510 298 5772

Module Characteristics

Table 1 – Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	85	ºC
Supply Voltage	V_{CC}	-0.5	3.6	V
Relative Humidity (non-condensing)	RH	5	95	%
Data Input Voltage Differential	IVDIP-VDINI	-	1	V
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V
Control Output Current	I_O	-20	20	mA

Table 2 – Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Operating Case Temperature	T_{OPR}	0	-	70	ºC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	ICC_IP	-	-	2200	mA	1
Sustained peak current at hot plug	ICC_SP	-	-	1815	mA	
Maximum Power Dissipation	P_D	-	-	5.5	W	
Maximum Power Dissipation, Low Power Mode	PDLP	-	-	1.5	W	
Aggregate Bit Rate	ABR	-	103.125	-	Gb/s	
Data Rate per Lane	DRL	-	25.78	-	Gb/s	
Control Input Voltage High	V_{IH}	V_{CC}*0.7	-	V_{CC}+0.3	V	
Control Input Voltage Low	V_{IL}	-0.3	-	V_{CC}*0.3	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Module power supply noise tolerance 10 Hz - 10 MHz (peak-to-peak)	-	-	-	66	mVpp	
Rx Differential Data Output Load	-	-	100	-	ohms	
Operating Distance	-	2	-	80,000	m	Note

Note: 40km without FEC and 80km with FEC.

Functional Characteristics (Optical)

The following tables list the performance specifications for the various functional blocks of the integrated optical transceiver module.

Table 3 – Transmitter Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit
Wavelength L0	λ_{C0}	1294.53	1295.56	1296.59	nm
Wavelength L1	λ_{C1}	1299.02	1300.05	1301.09	nm
Wavelength L2	λ_{C2}	1303.54	1304.58	1305.63	nm
Wavelength L3	λ_{C3}	1308.09	1309.14	1310.19	nm
Side-mode suppression ratio	SMSR	30			dB
Total Average Optical Launch Power	POUT	-	-	12.5	dBm
Average Launch Power Tx_Off (Each Lane)	POUT_OFF	-	-	-30	dBm
Average Optical Launch Power (Each Lane)	POUTL	2	-	6.5	dBm
Extinction Ratio	ER	6	-	-	dB
Spectral Width	Δλ	-	-	1	nm
Optical Modulation Amplitude (Each Lane)	OMA	2.5	-	7	dBm
Transmitter and Dispersion Penalty (Each Lane)	TDP	-	-	2.2	dB
Launch Power in OMA minus TDP (Each Lane)	OMA-TDP	1.5	-	-	dBm
Difference in launch power between any two lanes (OMA)	DT_OMA	-	-	4	dB
Optical Return Loss Tolerance	ORLT	-	-	20	dB
$RIN_{20}OMA$	RIN	-	-	-130	dB/Hz
Transmitter Reflectance	T_R	-	-	-26	dB
Transmitter Eye Mask Definition	-	IEEE 802.3bs-2010 {0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			

Table 4 – Receiver Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Wavelength L0	λ_{C0}	1294.53	1295.56	1296.59	nm	
Wavelength L1	λ_{C1}	1299.02	1300.05	1301.09	nm	
Wavelength L2	λ_{C2}	1303.54	1304.58	1305.63	nm	
Wavelength L3	λ_{C3}	1308.09	1309.14	1310.19	nm	
Receiver Sensitivity (OMA) per Lane				-27.5	dBm	Note
Stressed Receiver Sensitivity in OMA (Each Lane)	-	-	-	TBD	dBm	
Stressed Receiver Sensitivity Test Conditions:						
Stressed Eye J2 Jitter (Each Lane)	-	-	0.33	-	UI	
Stressed Eye J9 Jitter (Each Lane)	-	-	0.48	-	UI	
Vertical Eye Closure Penalty	-	-	2	-	dB	
Damage Threshold for Receiver	Pin, damage	TBD	-	-	dBm	
Average Receive Power (Each Lane)	-	-28	-	-5	dBm	Note
Receive Power in OMA (Each Lane), Overload	OMA	-	-	-4.5	dBm	
Receiver Reflectance	RX_R	-	-	-26	dB	
LOS Assert	LOSA	-40	-	-	dBm	
LOS De-assert	LOSD	-	-	-30	dBm	
LOS hysteresis	LOSH	0.5	-	-	dB	

Note: Measured with conformance test signal at TP3 for the BER = $5x10^{-5}$

Functional Characteristics (Electrical)

Table 5 – Electrical Specification

High-Speed Signal: Compliant to IEEE802.3 CAUI-4 C2M

Low-Speed Signal: Compliant to SFF-8679

Receiver (Module Output)						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Note**
Differential Data Input Amplitude	VIN,P-P	95	-	900	mVpp	
Differential Termination Mismatch		-	-	10	%	
LPMode, Reset and ModSelL	V_{IL}	-0.3	-	0.8	V	
	V_{IH}	2	-	V_{CC}+0.3	V	
Transmitter (Module Input)						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Note**
Differential Data Output Amplitude	VOUT,P-P	-	-	900	mVpp	
Differential Termination Mismatch		-	-	10	%	
Output Rise/Fall Time, 20%~80%	T_R	12	-	-	ps	
ModPrsL and IntL	V_{OL}	0	-	0.4	V	I_{OL}=4mA
	V_{OH}	V_{CC}-0.5	-	V_{CC}+0.3	V	I_{OL}=-4mA

Pin Definition

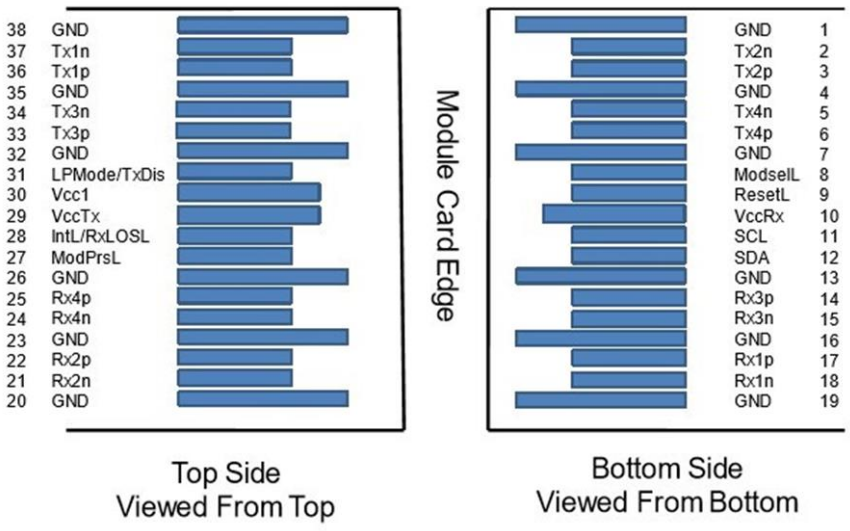

Figure 1 – Pinout definitions of QSFP28 module inputs/outputs

Table 7 – Module Pin Definitions

Pin	Logic	Symbol	Description	Plug Sequence	Note
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModselL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/RxLOS L	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636). Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636).	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode/TxDis	Low Power Mode. Optionally configurable as TxDis via the management interface (SFF-8636).	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
Note 2: VccRx, Vcc1 and VccTx are applied concurrently and may be internally connected within the module in any combination. Vcc contacts in SFF-8662 and SFF-8672 each have a steady state current rating of 1 A.

Recommended Host Board Power Supply Filtering

See SFF-8679

Table 8 – Timing for Soft Control and Status Functions

Parameter	Symbol	Min.	Max.	Unit
Initialization Time	t_init	-	TBD	s
Reset Init Assert Time	t_reset_init	10	-	µs
Serial Bus Hardware Ready Time	t_serial	-	2000	ms
Monitor Data Ready Time	t_data	-	2000	ms
Reset Assert Time	t_reset	-	2	s
LPMode Assert Time	ton_LPMode	-	100	ms
LPMode De-assert Time	toff_LPMode	-	300	ms
IntL Assert Time	ton_IntL	-	200	ms
IntL Deassert Time	toff_IntL	-	500	µs
RxLOSL Assert Time (Optional Fast Mode)	ton_f_LOS	-	1	ms
RxLOSL Deassert Time (Optional Fast Mode)	toff_f_LOS	-	3	ms
Rx LOS Assert Time	ton_lol	-	100	ms
Tx Fault Assert Time	ton_Txfault	-	200	ms
Flag Assert Time	ton_flag	-	200	ms
Mask Assert Time	ton_mask	-	100	ms
Mask Deassert Time	toff_mask	-	100	ms
Application or Rate Select Change Time	t_ratesel	-	N/A	ms
Power_over-ride or Power-set Assert Time	ton_Pdown	-	100	ms
Power_over-ride or Power-set De-assert Time	toff_Pdown	-	300	ms

Table 9 – I/O Timing for Squelch and Disable

Parameter	Symbol	Min.	Max.	Unit
Rx Squelch Assert Time	ton_Rxsq	-	15	ms
Rx Squelch Deassert Time	toff_Rxsq	-	15	ms
Tx Squelch Assert Time	ton_Txsq	-	400	ms
Tx Squelch Deassert Time	toff_Txsq	-	400	ms
Tx Disable Assert Time (fast mode)	ton_Txdisf	-	3	ms
Tx Disable Deassert Time (fast mode)	toff_Txdisf	-	10	ms
Rx Output Disable Assert Time	ton_Rxdis	-	100	ms
Rx Output Disable Deassert Time	toff_Rxdis	-	100	ms
Squelch Disable Assert Time	ton_sqdis	-	100	ms
Squelch Disable Deassert Time	toff_sqdis	-	100	ms

Parameter	Symbol	Min.	Max.	Unit
Rx Squelch Assert Time	ton_Rxsq	-	15	ms
Rx Squelch Deassert Time	toff_Rxsq	-	15	ms
Tx Squelch Assert Time	ton_Txsq	-	400	ms
Tx Squelch Deassert Time	toff_Txsq	-	400	ms

Parameter	Symbol	Min.	Max.	Unit
Tx Disable Assert Time (fast mode)	ton_Txdisf	-	3	ms
Tx Disable Deassert Time (fast mode)	toff_Txdisf	-	10	ms
Rx Output Disable Assert Time	ton_Rxdis	-	100	ms
Rx Output Disable Deassert Time	toff_Rxdis	-	100	ms
Squelch Disable Assert Time	ton_sqdis	-	100	ms
Squelch Disable Deassert Time	toff_sqdis	-	100	ms

Table 10 – Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to V_{CC}	±3%	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	2 to +6.5	±3	dB	Internal
Rx Receive Power (Each Lane)	-28 to -5	±3	dB	Internal

Mechanical Diagram